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3. **Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs**
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Paulos, J.J.; Antoniadis, D.A.;
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Azzopardi, S.; Vinassa, J.-M.; Woirgard, E.; Zardini, C.; Briat, O.;
Power Electronics, IEEE Transactions on
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20. **New generation 1200 V power module with trench gate IGBT and super soft recovery diode**
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Electric Power Applications, IEE Proceedings-
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Circuits, Devices and Systems, IEE Proceedings G
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1 A static power model for architects
J. Adam Butts, Gurindar S. Sohi
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture MICRO 33**
Publisher: ACM Press
Full text available: pdf(136.88 KB) ps(431.76 KB) Publisher Site
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2 Double-gate SOI devices for low-power and high-performance applications
K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, T. Cakici
May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**
Publisher: IEEE Computer Society
Full text available: pdf(783.31 KB) Additional Information: full citation, abstract

Double-gate (DG) transistors have emerged as promising devices for nano-scale circuits due to their better scalability compared to bulk CMOS. Among the various types of DG devices, quasi-planar SOI FinFETs are easier to manufacture compared to planar double-gate devices. DG devices with independent gates (separate contacts to back and front gates) have recently been developed. DG devices with symmetric and asymmetric gates have also been demonstrated. Such device options have direct implications ...

3 From Electron Mobility to Logical Structure: A View of Integrated Circuits
Wesley A. Clark
September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3
Publisher: ACM Press
Full text available: pdf(3.29 MB) Additional Information: full citation, references, citings, index terms

4 Power reduction techniques for microprocessor systems
Vasanth Venkatachalam, Michael Franz
September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3

Publisher: ACM Press
Full text available: pdf(602.33 KB) Additional Information: full citation, abstract, references, index terms

Power consumption is a major factor that limits the performance of computers. We survey the "state of the art" in techniques that reduce the total power consumed by a microprocessor system over time. These techniques are applied at various levels ranging from circuits to architectures, architectures to system software, and system software to applications. They also include holistic approaches that will become more important over the next decade. We conclude that power management is a ...

Keywords: Energy dissipation, power reduction

5 Managing leakage power: Analysis and minimization techniques for total leakage considering gate oxide leakage
Dongwoo Lee, Wesley Kwong, David Blaauw, Dennis Sylvester
June 2003 **Proceedings of the 40th conference on Design automation DAC '03**
Publisher: ACM Press
Full text available: pdf(217.28 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we address the growing issue of gate oxide leakage current (Igate) at the circuit level. Specifically, we develop a fast approach to analyze the total leakage power of a large circuit block, considering both Igate and subthreshold leakage (Isub). The interaction between Isub and Igate complicates analysis in arbitrary CMOS topologies and we propose simple and accurate heuristics based on table look-ups to quickly estimate the state-dependent total leakage current within 1% of SPICE ...

6 Delay optimization of combinational static CMOS logic
M. Hofmann, J. K. Kim
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation DAC '87**
Publisher: ACM Press
Full text available: pdf(864.63 KB) Additional Information: full citation, abstract, references, citings, index terms

Several methods for increasing the speed of combinational static CMOS circuits, including techniques for partitioning gates on the basis of circuit complexity and input arrival time, are described. The target layout style is standard cell, rather than a PLA or gate matrix scheme. Use of a standard-cell-like image allows a two-level buffered hierarchy to be introduced which is beneficial to reducing circuit delays. Preliminary results from device sizing algorithms are also given. The device ...

7 Is nanoelectronics the future of microelectronics?
Mark Lundstrom
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design ISLPED '02**
Publisher: ACM Press
Full text available: pdf(241.10 KB) Additional Information: full citation, abstract, references, index terms

We examine current research in nanoelectronics and discuss the role it may play in future electronic systems.

Keywords: Moore's Law, molecular electronics, nanoelectronics

8 Deep Sub-Micron IDDQ Testing: Issues and Solutions
M. Sachdev
March 1997 **Proceedings of the 1997 European conference on Design and Test EDTC '97**
Publisher: IEEE Computer Society
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, citings
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The effectiveness of I/sub DDQ/ testing in deep sub-micron is threatened by the increased transistor sub-threshold leakage current. In this article, we survey possible solutions and propose a deep sub-micron I/sub DDQ/ test mode. The methodology provides means for unambiguous measurements of I/sub DDQ/ components and defect diagnosis. The effectiveness of the test mode is demonstrated with a real life example.

Keywords: CMOS integrated circuits, deep submicron IDDQ testing, transistor sub-threshold leakage current, defect diagnosis, CMOS IC

9 Layout tools for analog ICs and mixed-signal SoCs: a survey
Rob A. Rutenbar, John M. Cohn
May 2000 **Proceedings of the 2000 international symposium on Physical design ISPD '00**
Publisher: ACM Press
Full text available: pdf(247.03 KB) Additional Information: full citation, references

10 Emerging technologies and designs for low power: Analysis of super cut-off transistors for ultralow power digital logic circuits
Arijit Raychowdhury, Xuanyao Fong, Qikai Chen, Kaushik Roy
October 2006 **Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06**
Publisher: ACM Press
Full text available: pdf(340.59 KB) Additional Information: full citation, abstract, references, index terms

Super cut-off devices with sub-60mV/decade subthreshold swings have recently been demonstrated and being extensively studied. This paper presents a feasibility analysis of such tunneling devices for ultralow power subthreshold logic. Analysis shows that this device can deliver 800X higher performance (@iso-IOFF) compared to a MOSFET. The possible use of this device as a sleep transistor in conjunction with the regular Si MOSFET shows 2000X average improvement in leakage power compared to Si MOSF ...

Keywords: carbon nanotube FETs, tunneling transistors

11 Spin MOSFETs as a basis for spintronics
Satoshi Sugahara, Masaaki Tanaka
May 2006 **ACM Transactions on Storage (TOS)**, Volume 2 Issue 2
Publisher: ACM Press
Full text available: pdf(427.11 KB) Additional Information: full citation, abstract, references, index terms

This article reviews a recently proposed new class of spin transistors referred to as spin metal-oxide-semiconductor field-effect transistors (spin MOSFETs), and their integrated circuit applications. The fundamental device structures, operating principle, and theoretically predicted device performance are presented. Spin MOSFETs potentially exhibit significant magnetotransport effects, such as large magneto-current, and also satisfy important requirements for integrated circuit applications suc ...

Keywords: MOSFETs, Spintronics, spin MOSFETs, spin transistors

12 Technologies and devices for low power: Modeling and analysis of total leakage currents in nanoscale double gate devices and circuits
Saibal Mukhopadhyay, Keunwoo Kim, Ching-Te Chuang, Kaushik Roy
August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**
Publisher: ACM Press
Full text available: pdf(485.85 KB) Additional Information: full citation, abstract, references, index terms

In this paper we model (numerically and analytically) and analyze sub-threshold, gate-to-channel tunneling, and edge direct tunneling leakage in Double Gate (DG) devices. We compare the leakage of different DG structures, namely, doped body symmetric device with polysilicon gates, intrinsic body symmetric device with metal gates and intrinsic body asymmetric device with different front and back gate material. It is observed that, use of (near-mid-gap) metal gate and intrinsic body devices signif ...

Keywords: SRAM, double-gate devices, estimation, gate leakage, quantum effect, stacking effect, subthreshold leakage

13 Low power circuits and microarchitectures: Utilizing reverse short channel effect for optimal subthreshold circuit design
Tae-Hyoung Kim, Hanyong Eom, John Keane, Chris Kim
October 2006 **Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06**
Publisher: ACM Press
Full text available: pdf(1.93 MB) Additional Information: full citation, abstract, references, index terms

The impact of the Reverse Short Channel Effect (RSCE) on device current is stronger in the subthreshold region due to the reduced Drain-Induced-Barrier-Lowering (DIBL) and the exponential dependency of current on threshold voltage. This paper describes a device size optimization method for subthreshold circuits utilizing RSCE to achieve high drive current, low device capacitance, less sensitivity to random dopant fluctuations, and better subthreshold swing. Simulation results using ISCAS benchma ...

Keywords: PVT variations, digital circuits, optimization, reverse short channel effect, subthreshold circuits, subthreshold operation

14 Power minimization in IC design: principles and applications
Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

15 A set of programs for MOS design
G. Sakauye, A. Lubiw, J. Royle, R. Epplett, J. Twidale, E. Shew, E. Attfield, F. Brglez, P. Wilcox
June 1981 **Proceedings of the 18th conference on Design automation DAC '81**
Publisher: IEEE Press
Full text available: pdf(778.19 KB) Additional Information: full citation, abstract, references, citings, index terms

A set of programs used in the design of custom hand packed and standard cell MOS circuits is described. The programs cover logic simulation, filter analysis, circuit simulation, timing simulation, circuit extraction from layout, design tolerance checking, connectivity checking and user interface facilities. A cell documentation system is used to tie together the various design support packages.

16 Power optimization of large-scale circuits: Analysis and optimization of gate leakage current of power gating circuits
Hyung-Ock Kim, Youngsoo Shin
January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**
Publisher: ACM Press
Full text available: pdf(151.22 KB) Additional Information: full citation, abstract, references

Power gating is widely accepted as an efficient way to suppress subthreshold leakage current. Yet, it suffers from gate leakage current, which grows very fast with scaling down of gate oxide. We try to understand the sources of leakage current in power gating circuits and show that input MOSFETs play a crucial role in determining total gate leakage current. It is also shown that the choice of a current switch in terms of polarity, threshold voltage, and size has a significant impact on total lea ...

17 Challenges and design choices in nanoscale CMOS
Siva G. Narendra
March 2005 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: pdf(5.35 MB) Additional Information: full citation, abstract, references, index terms

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In this article, we will first review the history of technology scaling that follows Moore's law from the prespective of microprocessor designs. Challenges to continue the historical scaling trends will be highlighted and design choices to address two specific challenges, process variation and leakage power, will be discussed. In nanoscale CMOS technology generations, supply and thresh ...

Keywords: CMOS, leakage power, nanoscale, process variation

18 Low power digital circuits design: Total leakage power optimization with improved mixed gates
Frank Sill, Frank Grassert, Dirk Timmermann

September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and system design SBCCI '05**
Publisher: ACM Press
Full text available: pdf(288.69 KB) Additional Information: full citation, abstract, references, index terms

Gate oxide tunneling current Igate and sub-threshold current Isub dominate the leakage of designs. The latter depends on threshold voltage Vth while Igate vary with the thickness of gate oxide layer Tox. In this paper, we propose a new method that combines approaches of Dual Threshold CMOS (DTCMOS), mixed-Tox CMOS, and pin-reordering. As the reduction of leakage leads to an increase of gate delay, our purpose is the reduction of total leakage at constant design performance. We modified a given t ...

Keywords: MVT, leakage currents, threshold voltage

19 Topological Analysis for Leakage Prediction of Digital Circuits
Wenjie Jiang, Vivek Tiwari, Erik de la Iglesia, Amit Sinha
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design ASP-DAC '02**
Publisher: IEEE Computer Society
Full text available: pdf(115.48 KB) Publisher Site Additional Information: full citation, abstract, citings

Subthreshold leakage current is becoming an increasingly significant portion of the power dissipation in microprocessors due to technology and voltage scaling. Techniques to estimate leakage at the full chip level are indispensable for power budget allocation. In addition, simple and practical approaches and rules of thumb are needed to allow leakage to become part of the vocabulary of all designers. This paper focuses on the impact of circuit topology on leakage, which is often abstracted throu ...

20 Session 32: logic synthesis I: Gate sizing: finFETs vs 32nm bulk MOSFETs
Brian Swahn, Soha Hassoun
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(800.60 KB) Additional Information: full citation, abstract, references, index terms

FinFET devices promise to replace traditional MOSFETs because of superior ability in controlling leakage and minimizing short channel effects while delivering a strong drive current. We investigate in this paper gate sizing of finFET devices, and we provide a comparison with 32nm bulk CMOS. Wider finFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the finFET's double gates allows significant reduction in leakage current. We perform temper ...

Keywords: FinFET, gate sizing, thermal modeling

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#2	insulated<sentence>transistor? and evaluat*<paragraph>transistor?
#3	((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<AND>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata))
#4	((((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)))<AND>((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)) and channel width)
#5	((((((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)))<and>((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)) and channel width))<AND>((((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)))<and>((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)) and channel width) and threshold voltage)
#6	((((((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)))<and>((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)) and channel width))<AND>((((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)))<and>((insulated<sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat*<paragraph>transistor?<in>metadata)) and channel width) and threshold voltage)
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#8	insulated gate<sentence>transistor? and drain current method?
#9	insulated gate<sentence>transistor? and drain current method?

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☐ 1. Document ID: US 20040098681 A1

L1: Entry 1 of 9 File: PGPB May 20, 2004

PGPUB-DOCUMENT-NUMBER: 20040098681
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040098681 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: May 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 2. Document ID: US 20030113946 A1

L1: Entry 2 of 9 File: PGPB Jun 19, 2003

PGPUB-DOCUMENT-NUMBER: 20030113946
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030113946 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: June 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 438/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20020130679 A1

L1: Entry 3 of 9 File: PGPB Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020130679
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020130679 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 324/769

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20020127749 A1

L1: Entry 4 of 9 File: PGPB Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020127749
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020127749 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 438/18; 438/17, 438/275

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6727724 B2

L1: Entry 5 of 9 File: USPT Apr 27, 2004

US-PAT-NO: 6727724
DOCUMENT-IDENTIFIER: US 6727724 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6649430 B2

L1: Entry 6 of 9 File: USPT Nov 18, 2003

US-PAT-NO: 6649430
DOCUMENT-IDENTIFIER: US 6649430 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 438/17; 438/275

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6559672 B2

L1: Entry 7 of 9 File: USPT May 6, 2003

US-PAT-NO: 6559672
DOCUMENT-IDENTIFIER: US 6559672 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: May 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6373274 B1

L1: Entry 8 of 9 File: USPT Apr 16, 2002

US-PAT-NO: 6373274
DOCUMENT-IDENTIFIER: US 6373274 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6169415 B1

L1: Entry 9 of 9 File: USPT Jan 2, 2001

US-PAT-NO: 6169415
DOCUMENT-IDENTIFIER: US 6169415 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: January 2, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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TYPES	1668490

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☐	L1	insulated gate type transistor	263

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Search Results - Record(s) 1 through 12 of 12 returned.

☐ 1. Document ID: US 20040098681 A1

L2: Entry 1 of 12 File: PGPB May 20, 2004

PGPUB-DOCUMENT-NUMBER: 20040098681
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040098681 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: May 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 716/4

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De

☐ 2. Document ID: US 20040037148 A1

L2: Entry 2 of 12 File: PGPB Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040037148
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040037148 A1

TITLE: MIS semiconductor device having improved gate insulating film reliability

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hidaka, Hideto	Hyogo		JP

US-CL-CURRENT: 365/223

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De

☐ 3. Document ID: US 20030113946 A1

L2: Entry 3 of 12 File: PGPB Jun 19, 2003

PGPUB-DOCUMENT-NUMBER: 20030113946
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030113946 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: June 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 438/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20020130679 A1

L2: Entry 4 of 12 File: PGPB Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020130679
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020130679 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 324/769

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 20020127749 A1

L2: Entry 5 of 12 File: PGPB Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020127749
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020127749 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Yamaguchi, Kenji	Tokyo		JP

US-CL-CURRENT: 438/18; 438/17, 438/275

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 20020024059 A1

L2: Entry 6 of 12 File: PGPB Feb 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020024059
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020024059 A1

TITLE: MIS semiconductor device having improved gate insulating film reliability

PUBLICATION-DATE: February 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hidaka, Hideto	Hyogo		JP

US-CL-CURRENT: 257/189

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6816418 B2

L2: Entry 7 of 12 File: USPT Nov 9, 2004

US-PAT-NO: 6816418
DOCUMENT-IDENTIFIER: US 6816418 B2

TITLE: MIS semiconductor device having improved gate insulating film reliability

DATE-ISSUED: November 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hidaka; Hideto	Hyogo			JP

US-CL-CURRENT: 365/189.09; 365/185.23, 365/201, 365/226

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6727724 B2

L2: Entry 8 of 12 File: USPT Apr 27, 2004

US-PAT-NO: 6727724
DOCUMENT-IDENTIFIER: US 6727724 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6649430 B2
L2: Entry 9 of 12 File: USPT Nov 18, 2003

US-PAT-NO: 6649430
DOCUMENT-IDENTIFIER: US 6649430 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 438/17; 438/275

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 10. Document ID: US 6559672 B2
L2: Entry 10 of 12 File: USPT May 6, 2003

US-PAT-NO: 6559672
DOCUMENT-IDENTIFIER: US 6559672 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: May 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 11. Document ID: US 6373274 B1

L2: Entry 11 of 12 File: USPT Apr 16, 2002

US-PAT-NO: 6373274
DOCUMENT-IDENTIFIER: US 6373274 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 12. Document ID: US 6169415 B1

L2: Entry 12 of 12 File: USPT Jan 2, 2001

US-PAT-NO: 6169415
DOCUMENT-IDENTIFIER: US 6169415 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: January 2, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yamaguchi; Kenji	Tokyo			JP

US-CL-CURRENT: 324/769; 324/719

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Term	Documents
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EVALUAT	26
EVALUATABILITY	7